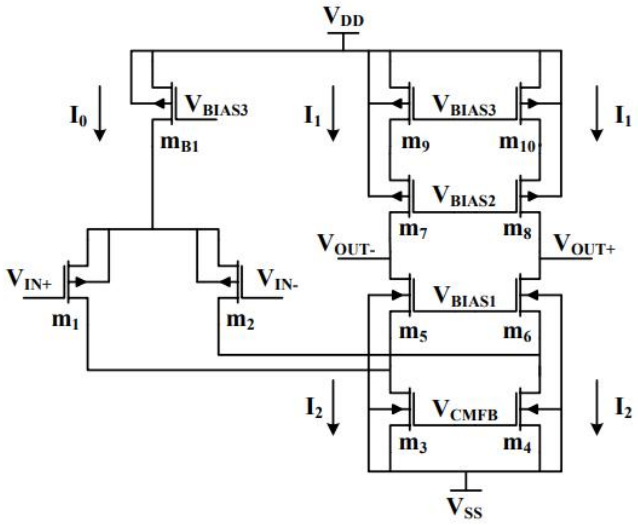
Family Name: _____ **First Name:** _____.

Test 8h15/10h45

LP Analog Design – Final Exam (Mock)

1. Fully differential folded cascode OTA: Procedural sizing

The purpose of this section is to provide the sizing procedure of the following OTA step-by-step. Starting by choosing circuit-level parameters (specifications) and propagating them to transistor level.



The technology used is UMC 180nm 1.8V devices and their parameters are:

Parameter		Unit Extracted	
K_p	PMOS	52	µA/V²
	NMOS	250	
U_a	PMOS	16	V/µm
	NMOS	5	
n	PMOS	1.3	-
	NMOS	1.2	
C_{ox}		8.3	fF/µm²

The OTA, have to meet the following specifications.

Parameter	Value Specification		Unit
Open-loop gain	> 70		dB
GBW	60		MHz
Slew rate [**SR**]	50		V/µs
Load capacitors [C_L]	100		fF

8h15/10h45

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Value	Unit	Guideline
	µA	From SR
	µA	

the differential pair.

	Unit	Guideline
	μS	From GBW
	-	From $\frac{g_{m2}}{I_{D2}}$
	-	From I_{f2}

ized.

ion factor: **I_F= 10 or I_F = 1**.

Value	Unit	Guideline

8h15/10h45

Mock)

ification.

	Unit	Guideline
	MΩ	

), determine the conductance and length

$_{up} = R_{down}$)
f 85µm²)

Guideline
$R_{up} = R_{down} = 2R_{out}$
$L_9 = 2L_9$
$L_7 = 2L_9$
$R_{up} = R_{down} = 2R_{out}$

8h15/10h45

c)

$L_3 = 2L_5$
$L_3 = 2L_5$

Guideline

Guideline
$g_{ds1} \le 0.5 g_{ds3}$

Guideline

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hat include the

$\left(\frac{\partial I_D}{\partial V_{TO}}\right)^2$

$(g_m)^2$

e common-mode
scode OTA (i.e.

Family Name: _____ **First Name:** _____.

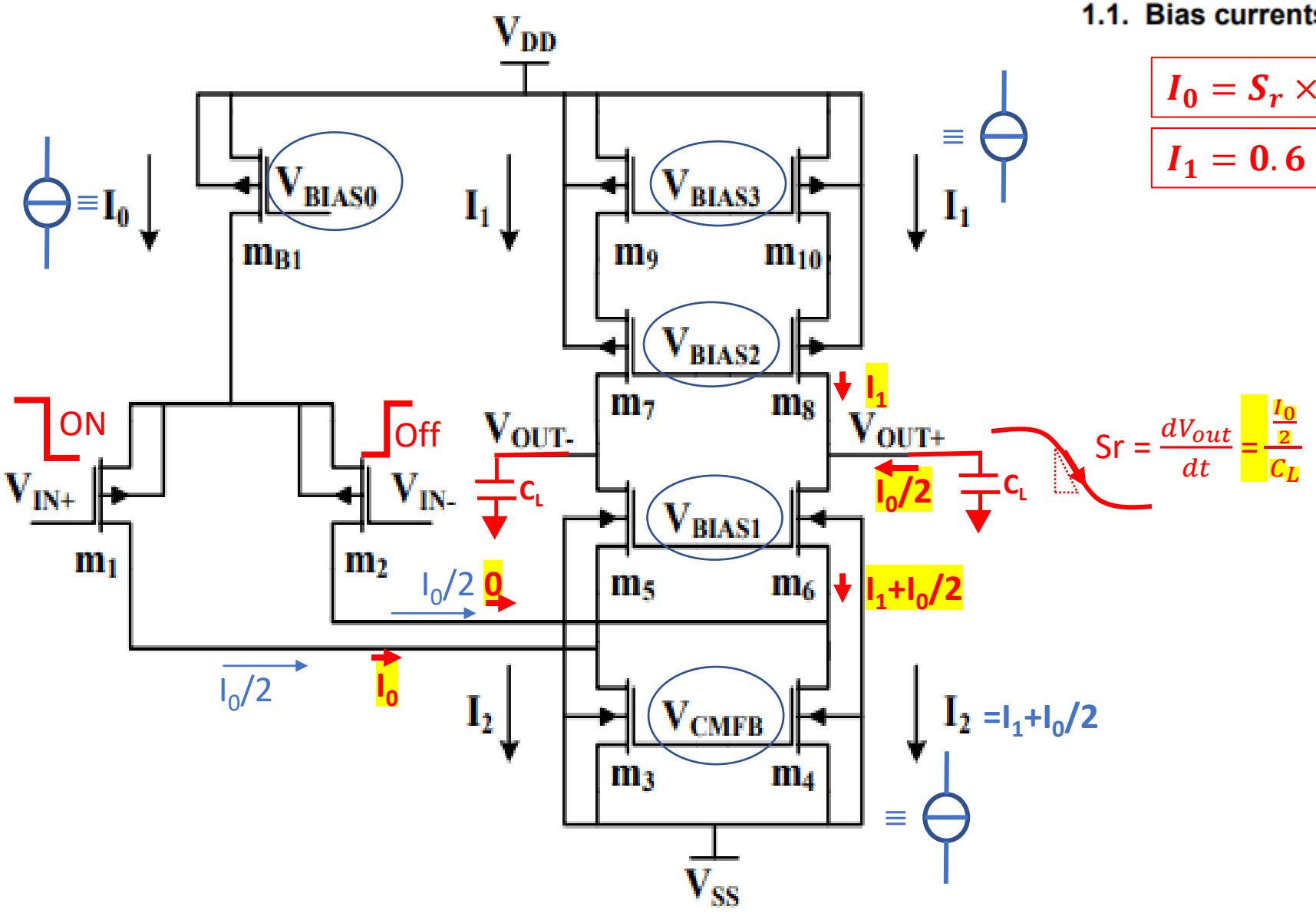
Test 8h15/10h45

LP Analog Design – Final Exam (Mock)

1.1. Bias currents

	Parameter	Expression	Value	Unit	Guideline
Bias	I_o			µA	From SR
	I_1	$\mathbf{1,2 \times \frac{I_o}{2}}$		µA	

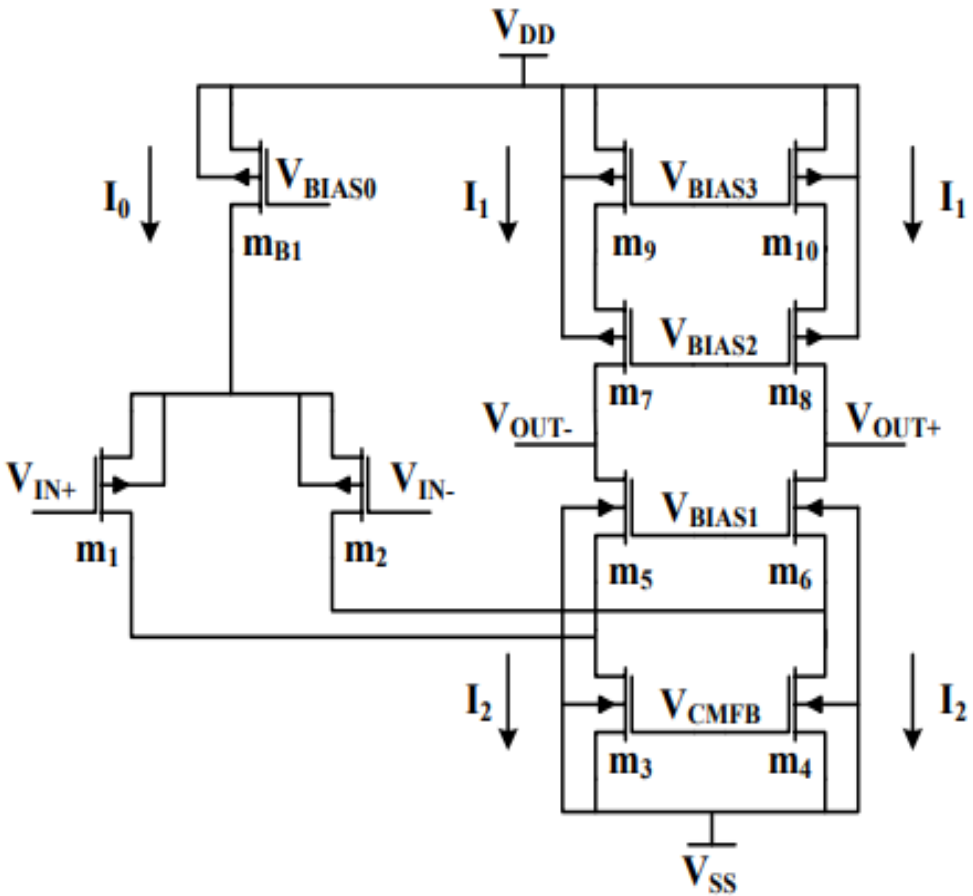
1. Fully differential folded cascode OTA: Procedural sizing



1.1. Bias currents

$I_0 = S_r \times 2C_L$ = 10 µA

$I_1 = 0.6 \times I_0$ = 6 µA



1.2. Differential pair

Determine the transconductance, inversion factor and W/L ratio of the differential pair.

	Parameter	Expression	Value	Unit	Guideline
Differential pair	$g_{m1,2}$			μS	From GBW
	$I_{f1,2}$			-	From $\frac{g_{m2}}{I_{D2}}$
	$\frac{W_{1,2}}{L_{1,2}}$			-	From I_{f2}

1.2. Differential pair

$$f_{gbw} = \frac{g_{m1,2}}{2 \times \pi \times C_L}$$

$$g_{m1,2} = f_{gbw} \times 2 \times \pi \times C_L = 38\ \mu S$$

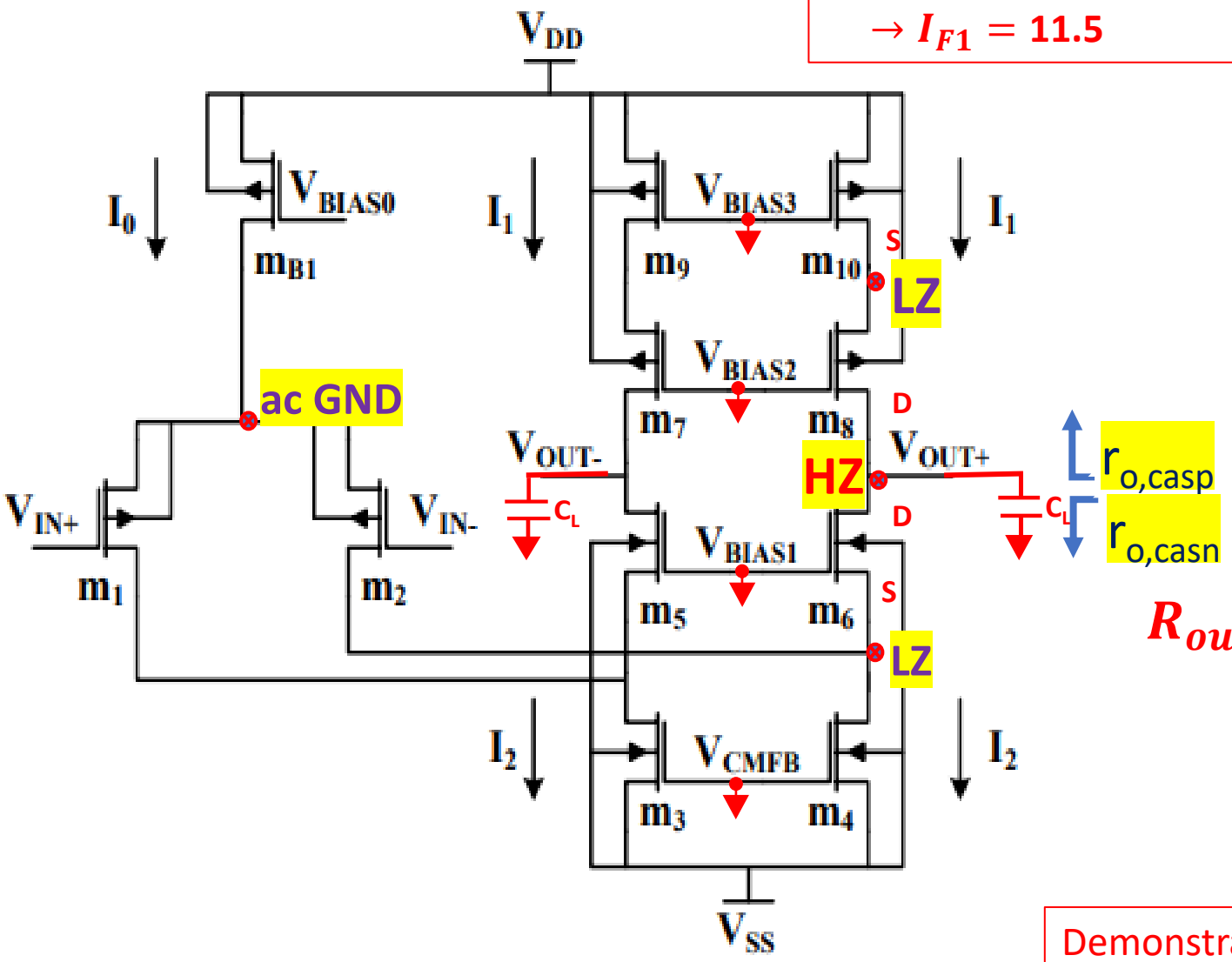
$$\frac{g_{m1}}{I_{D1}} = \frac{g_{m1}}{I_0/2} = \frac{1}{nU_T} \cdot \frac{2}{1 + \sqrt{4I_{F1} + 1}}$$

$$\rightarrow I_{F1} = 11.5$$

$$I_{F1} = \frac{I_{D1}}{2n\mu C_{ox} \frac{W}{L}\Big|_1 U_T^2}$$

$$\rightarrow \frac{W}{L}\Big|_1 = 4.8$$

Demonstration



$$f_{gbw} = |A_0| f_{p,dom}$$

(? over $|A_0|$; ? over $f_{p,dom}$)

$$f_{p,dom} = \frac{1}{2\pi R_{HZ} C_{HZ}} = \frac{1}{2\pi R_{out} C_L}$$

$$R_{out} = r_{o,casn} // r_{o,casp} \qquad A_0 = -g_{m2} R_{out}$$

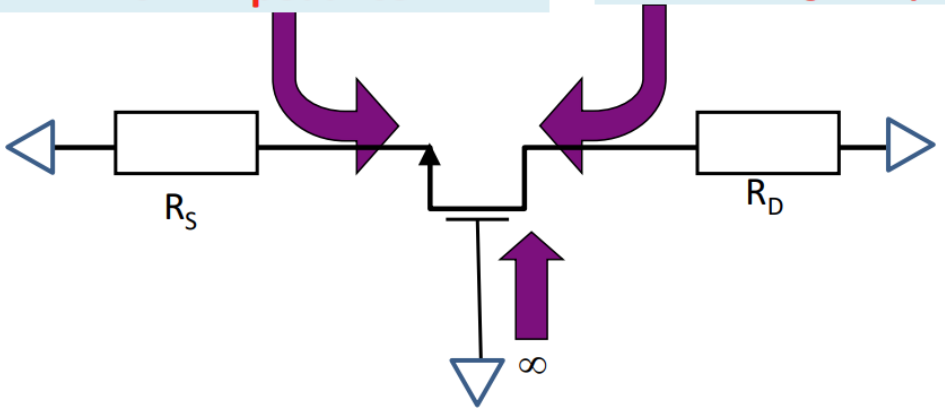
$$f_{gbw} = |A_0| f_{p,dom} = \frac{g_{m1,2}}{2 \times \pi \times C_L}$$

Demonstration of $A_0 = -g_{m2} R_{out}$

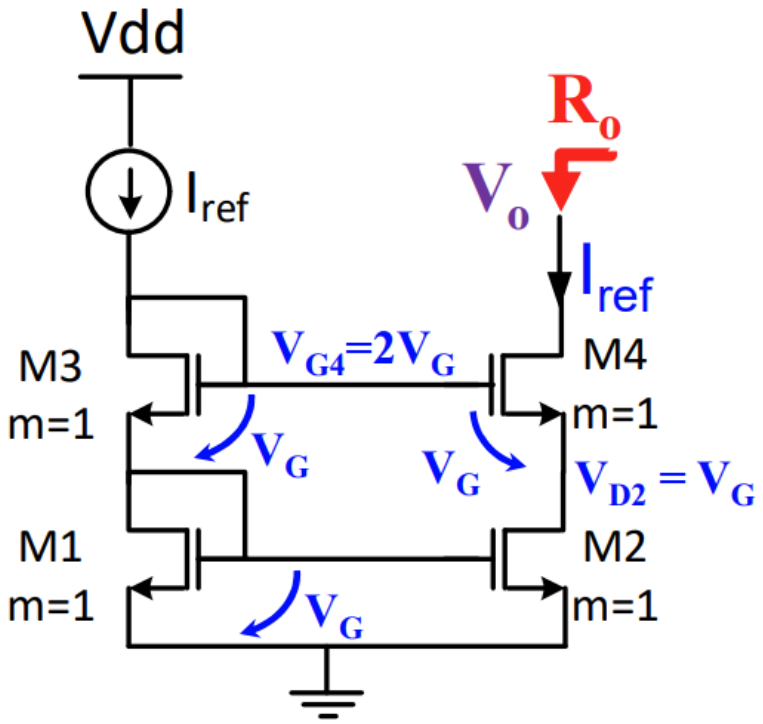
Course Review

$r_{is} = \frac{v_s}{-i_s} \approx \frac{1}{g_m + g_{ds}}(1 + R_D g_{ds})$ Low-impedance

$r_{id} = \frac{v_d}{i_d} = \frac{1}{g_{ds}}\left(1 + R_S(g_m + g_{ds})\right)$ High-impedance



- Cascode as active load

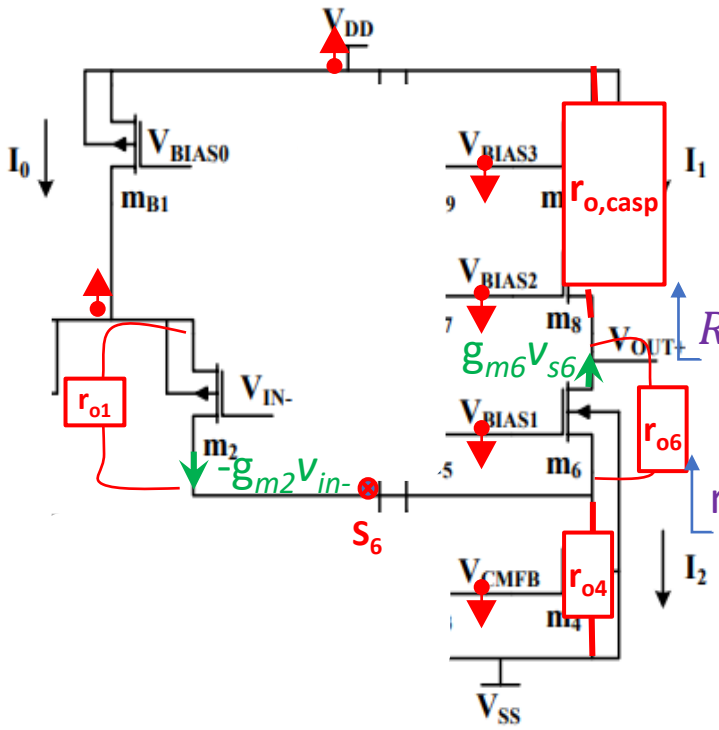


$$R_o = r_{o4}(1 + g_{m4}r_{o2}) \approx g_{m4}r_{o4}r_{o2}$$

Demonstration of $A_0 = -g_{m2}R_{out}$

$$A_0 = \frac{v_{out+}-v_{out-}}{v_{in-}-v_{in+}} = \frac{v_{out+}}{v_{in-}} = \frac{v_{out+}}{v_{s6}} \cdot \frac{v_{s6}}{v_{in-}}$$

Half circuit method



(Com_Source)

$$\frac{v_{s6}}{v_{in-}} = -\,g_{m2}(r_{o1}//r_{o4}//\overbrace{r_{o,s6}}^{?}) = -\,g_{m2}\,(r_{o1}//r_{o4}//\frac{1}{g_{m6}}(1+R_D g_{ds}))$$

$$\frac{v_{out+}}{v_{s6}} = g_{m6}\,(r_{o6}//r_{o,casp})\ \text{(Com\_Gate)}$$

$v_{out+}=(g_{m6}v_{s6} - i_{o6})r_{o,casp}$ with $i_{o6} = \frac{v_{out+}-v_{s6}}{r_{o6}}$

$R_D = r_{o,casp} = g_{m8}r_{o8}r_{o10}$

$g_{m6}v_{s6}$

$r_{o,s6} = \frac{1}{g_{m6}}(1+R_D r_{o6}^{-1})$

$$A_0 = -\,gm_2\,(\overbrace{ro_1//ro_4//\frac{1}{g_{m6}}(1+r_{o,casp}r_{o6}^{-1})}^{r_o^*})\cdot g_{m6}(ro_6//ro_{,casp})$$

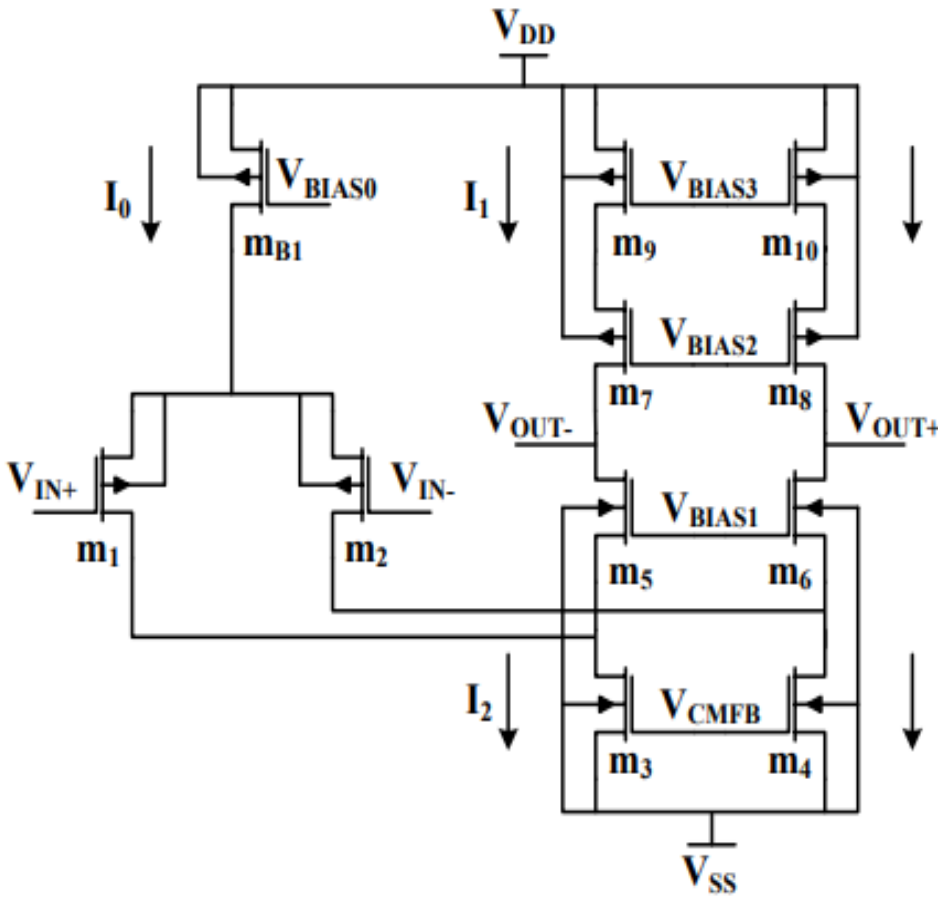
$$A_0 = -\,gm_2\,\frac{r_o^*\frac{1}{g_{m6}}(1+r_{o,casp}r_{o6}^{-1})}{r_o^*+\frac{1}{g_{m6}}(1+r_{o,casp}r_{o6}^{-1})}\cdot \times \frac{g_{m6}r_{o6}}{g_{m6}r_{o6}} \times \frac{g_{m6}r_{o6}r_{o,casp}}{r_{o6}+r_{o,casp}}$$

$$= -\,gm_2\,\frac{r_o^*(r_{o6}+r_{o,casp})}{g_{m6}r_{o6}r_o^*+r_{o6}+r_{o,casp}}\cdot \frac{g_{m6}r_{o6}r_{o,casp}}{r_{o6}+r_{o,casp}}$$

$$= -\,gm_2\,\frac{g_{m6}r_{o6}r_o^*\cdot r_{o,casp}}{g_{m6}r_{o6}r_o^*+r_{o,casp}} = -\,gm_2\,\overbrace{r_{o,casn}//r_{o.casp}}^{R_{out}}$$

$r_{o,casn}$

1.3. Folded cascade load



The 8 transistors composing the folded cascode stage will now be sized.
Determine the inversion factor and W/L ratio of these transistors to:

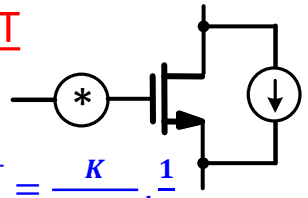
- Minimize the noise and offset (first priority)
- Keep saturation voltages of small (second priority))
- For simplification, only two values will be chosen for the inversion factor: $\mathbf{I_F = 10}$ **or** $\mathbf{I_F = 1}$.

	Parameter	Expression	Value	Unit	Guideline
Folded	$\frac{W_5}{L_5}$				
	$\frac{W_7}{L_7}$				
	$\frac{W_9}{L_9}$				
	$\frac{W_3}{L_3}$				

Course Review

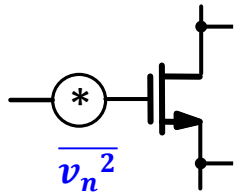
Cascode, Thermal noise

MOSFET



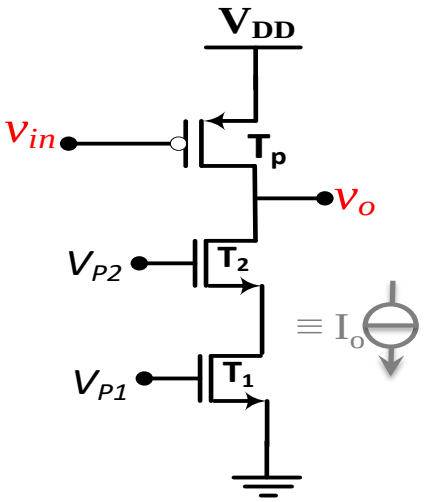
$\overline{i_n^2} = 4kT\gamma g_m$ (Thermal noise)

$\overline{v_n^2} = \frac{K}{C_{ox}LW}\cdot\frac{1}{f}$ (Flicker noise)



$\overline{v_n^2} = 4kT\gamma\frac{1}{g_m} + \frac{K}{C_{ox}LW}\cdot\frac{1}{f}$

(Thermal noise +Flicker noise)



$\overline{v_{n,o}^2}\big|_{T_2}$ negligible (degenerated CS: $\frac{v_o}{v_{pe}} \approx \frac{g_{m2}r_{op}}{1+g_{m2}r_{o1}} \approx \frac{r_{op}}{r_{o1}}$ close to1)

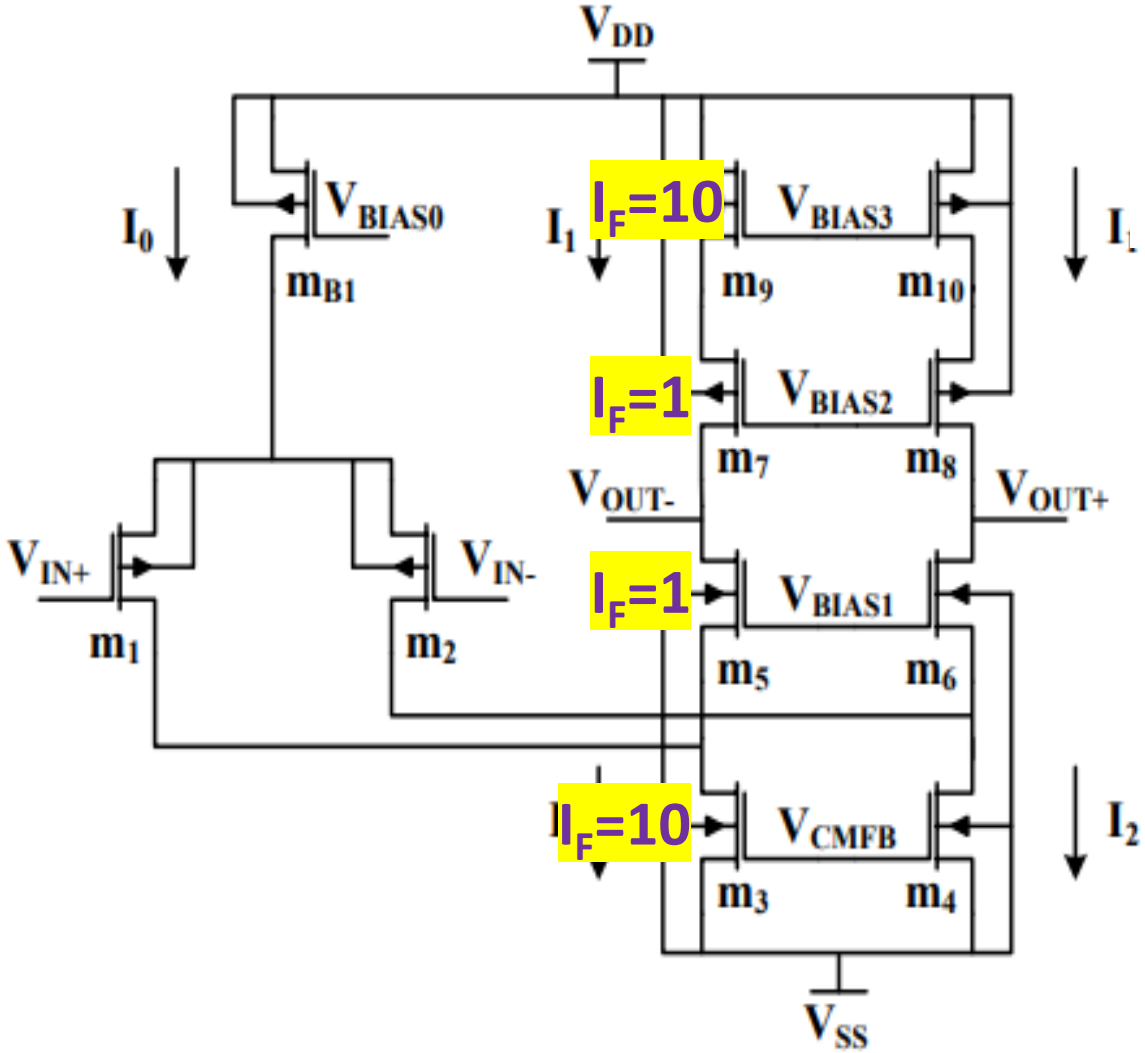
$$\overline{v_{n,o}^2}\big|_{T_1} = \left(4kT\gamma\frac{1}{g_{m1}}\right)(g_{m1}R_{out})^2$$

$$\overline{v_{n,i}^2} = 4kT\gamma\frac{1}{g_{mp}} + \left(4kT\gamma\frac{1}{g_{m1}}\right)\frac{(g_{m1}R_{out})^2}{(g_{mp}R_{out})^2}$$

$\overline{v_{n,i}^2}$ ↘ if g_{mp} (active T) ↗ ; and g_{m1} (Load T) ↘

⇒Active T in weak_Inversion ; and Load T in strong_Inversion

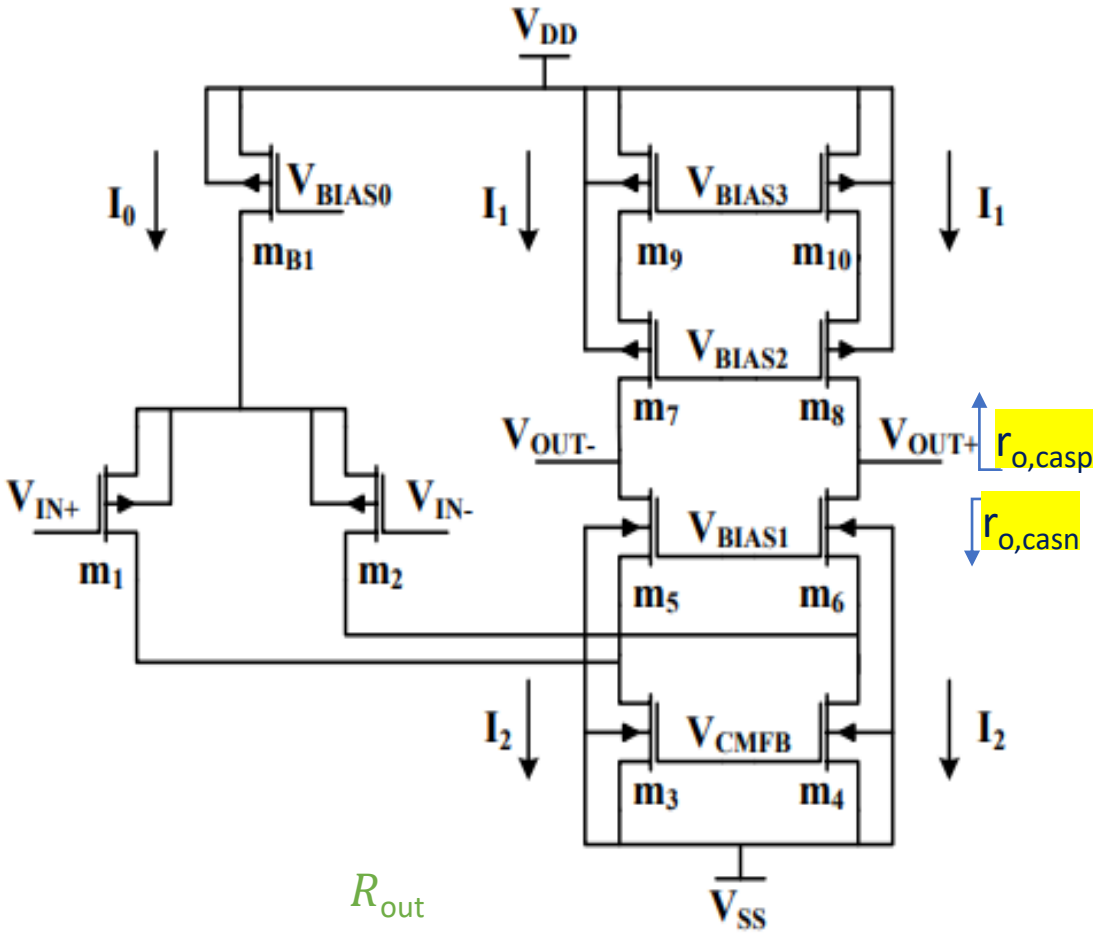
1.3. Folded cascode load



The 8 transistors composing the folded cascode stage will now be sized.
Determine the inversion factor and W/L ratio of these transistors to:

- Minimize the noise and offset (first priority)
- Keep saturation voltages of small (second priority))
- For simplification, only two values will be chosen for the inversion factor: **$I_F = 10$ or $I_F = 1$**..

	Parameter	Expression	Value	Unit	Guideline
Folded	$\frac{W_5}{L_5}$	$\frac{I_1}{2 \times n \times K_{p,n} \times I_{f5} \times u_T^2}$	15		Minimize saturation voltages $I_{f5} = 1$ save area
	$\frac{W_7}{L_7}$	$\frac{I_1}{2 \times n \times K_{p,p} \times I_{f7} \times u_T^2}$	64.1		Minimize saturation voltages $I_{f7} = 1$ save area
	$\frac{W_9}{L_9}$	$\frac{Id_9}{2 \times n \times K_p \times I_{f9} \times u_T^2}$	6.6		Minimize noise contribution $I_{f9} = 10$
	$\frac{W_3}{L_3}$	$\frac{Id_3}{2 \times n \times K_p \times I_{f3} \times u_T^2}$	2.8		Minimize noise contribution $I_{f3} = 10$ Operate in strong inversion



R_{out}

$A_0 = -gm_2\, r_{o,casn} // r_{o.casp}$

$r_{o,casp} = g_{m8} r_{o8}\, r_{o10}$

$r_{o,casn} = g_{m6} r_{o6} (r_{o4} // r_{o2})$

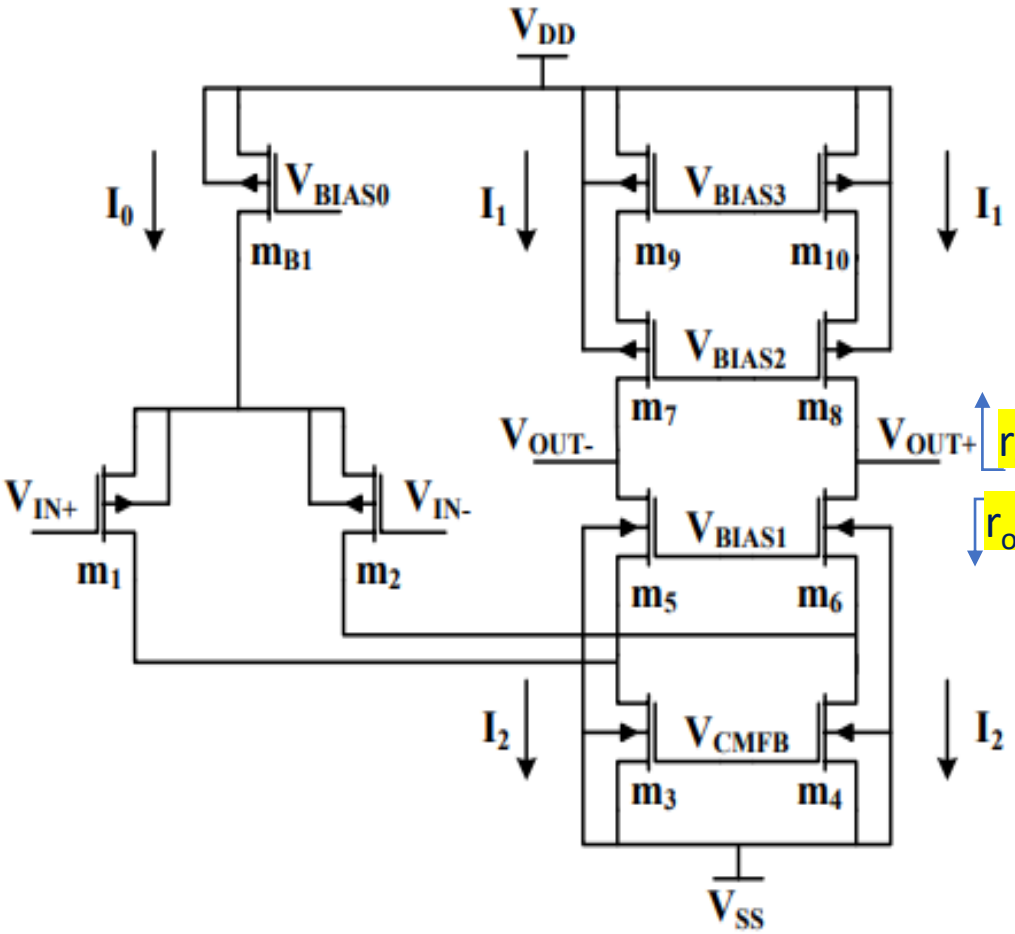
Calculate the output resistance necessary to meet the open-loop gain specification.

	Parameter	Expression	Value	Unit	Guideline
Rout	R_{out}			MΩ	

Neglecting the conductance of the differential pair (assume $g_{ds1} \approx 0.5 g_{ds3}$), determine the conductance and length of all transistors so that:

- The specified open-loop gain is achieved
- The NMOS and PMOS resistances at the output node are balanced ($R_{up} = R_{down}$)
- The total area of the folded cascade stage is minimized (in the order of 85µm^2)
  - m_7 and m_9 have the same length
  - The length of m_3 is two times the one of m_5

	Parameter	Expression	Value	Unit	Guideline
Rout	$n_n \times g_{m5,7}$			µS	
	R_{up}			MΩ	$R_{up} = R_{down} = 2R_{out}$
	$L_7 \times L_9$			µm^2	
	L_7			µm	$L_9 = 2L_9$
	L_7			µm	$L_7 = 2L_9$
	R_{down}			MΩ	$R_{up} = R_{down} = 2R_{out}$



$$r_{o,casn} = g_{m5} r_{o5} (r_{o3} // r_{o1})$$

$$r_{o,casp} = g_{m7} r_{o7}\, r_{o9}$$

$$A_0 = -gm_1 \left(R_{out}\right) = -gm_1 \left(r_{o,casn} // r_{o.casp}\right)$$

Calculate the output resistance necessary to meet the open-loop gain specification.

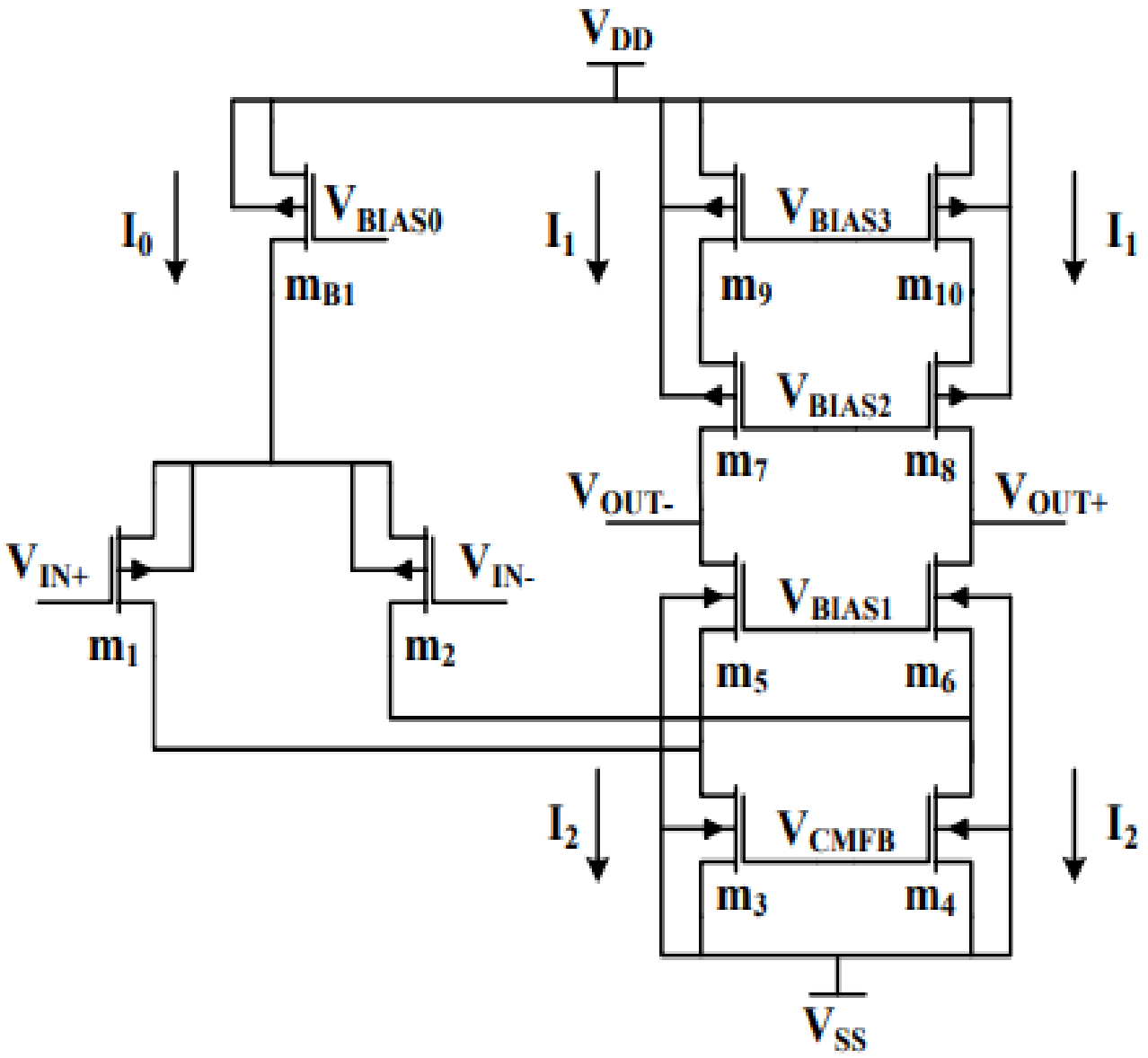
	Parameter	Expression	Value	Unit	Guideline
Rout	R_{out}	$\frac{A_0}{g_{m1,2}}$	84	MΩ	2

Neglecting the conductance of the differential pair (assume $g_{ds1} \approx 0.5 g_{ds3}$), determine the conductance and length of all transistors so that:

- The specified open-loop gain is achieved
- The NMOS and PMOS resistances at the output node are balanced ($R_{up} = R_{down}$)

	Parameter	Expression	Value	Unit	Guideline
Rout	$n_{np} \times g_{m5,7}$	$\frac{1}{u_T} \times \frac{2I_1}{1+\sqrt{1+4I_{f5,7}}}$	142.6	µS	
	R_{up}	$\frac{g_{m7}}{g_{ds7} \times g_{ds9}}$	168	MΩ	$R_{up} = R_{down} = 2R_{out}$ 1
	$L_7 \times L_9$	$\frac{2 \times R_{out} \times I_1^2}{n_p \times g_{m5,7} \times U_{ap}^2}$	0.2	µm²	
	L_7	$L_7 = \sqrt{0.5 \times L_7 \times L_9}$	0.3	µm	$L_9 = 2L_7$
	L_9	$= 2L_7$	0.6	µm	L_7 1
	R_{down}	$\frac{g_{m5}}{g_{ds5} \times (g_{ds1} + g_{ds3})}$	168	MΩ	$R_{up} = R_{down} = 2R_{out}$
	$L_3 \times L_5$	$\frac{1.5 \times 2 \times R_{out} \times I_{D3} \times I_{D5}}{n_n \times g_{m5} \times U_{an}^2}$	5.5	µm²	

1.5 Offset Estimation:

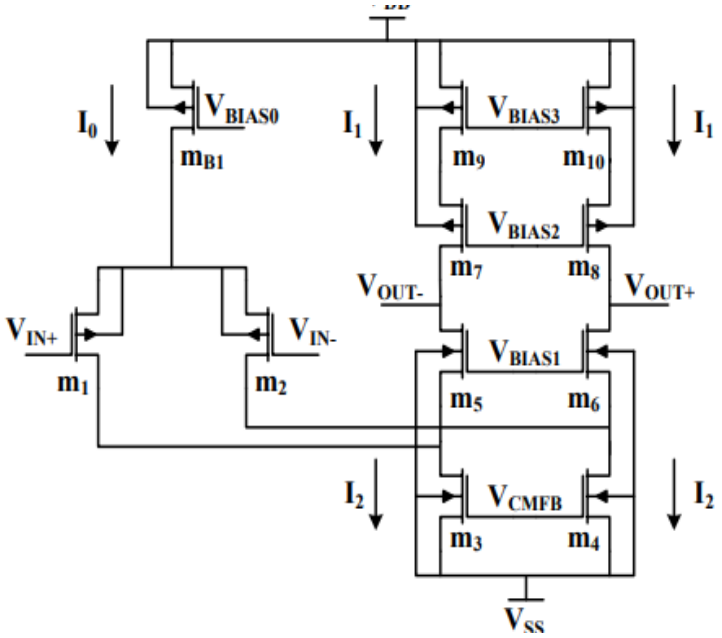


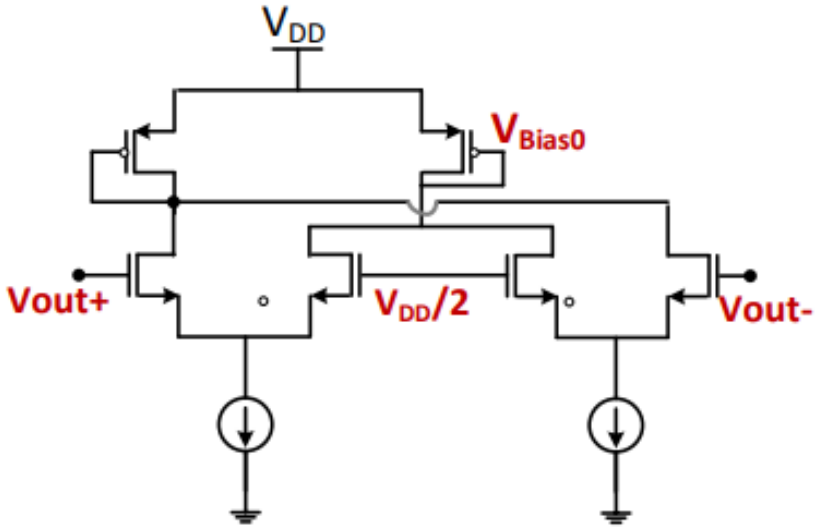
$$\sigma_{V_G(\beta,V_{T0})}{}^2 = \sigma_{V_{T0}}{}^2 + \left[\frac{I_D}{g_m}\right]^2 \left(\frac{\sigma_\beta}{\beta}\right)^2$$

$$\sigma_{Vos}{}^2 = \sigma_{VT}^2 + \left(\frac{I_0}{2gm_{1,2}}\right)^2 \left(\sigma'_{\beta 1,2}\right)^2 + \left(\frac{gm_{3,4}}{gm_{1,2}}\right)^2 \sigma_{VT}^2 + \left(\frac{I_{3,4}}{gm_{1,2}}\right)^2 \left(\sigma'_{\beta 3,4}\right)^2 + \left(\frac{gm_{9,10}}{gm_{1,2}}\right)^2 \sigma_{VT}^2 + \left(\frac{I_{9,10}}{gm_{1,2}}\right)^2 \left(\sigma'_{\beta 9,10}\right)^2$$

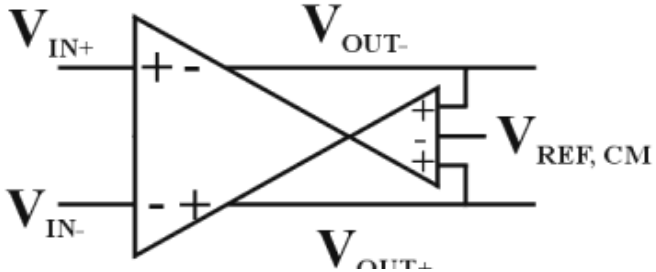
$$\sigma'_{\beta i} = \sigma_{\beta i}/\beta_i$$

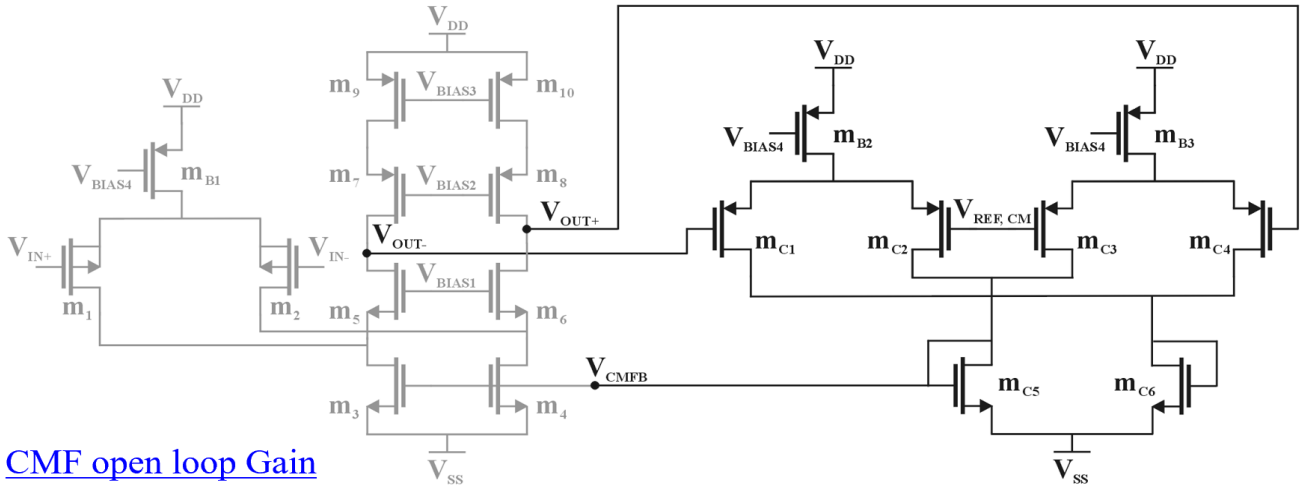
1.6 Common-mode feedback CMFB





Course Review





CMF open loop Gain

$$A_{CMFB} = \frac{\Delta v_{out,CM}}{\Delta v_{g,mc1,4}} = \frac{\Delta v_{out,CM}}{\Delta v_{CMFB}} \frac{\Delta v_{CMFB}}{\Delta v_{g,mc1,4}} = -g_{m,3,4} R_{out} \frac{g_{mc1,4}}{g_{mc5,6}}$$